

## **Metrology Roadmap 2009**

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**Japan**

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**Korea**

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**North America**

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# 2009 ITRS Changes

		2010	2012	2014	2016	2018
	<b>Flash 1/2 pitch (nm)</b>	32	25	20	16	13
	<b>DRAM ½ Pitch (nm)</b>	45	36	28	23	18.0
	<b>MPU Printed Gate Length (nm)</b>	41	31	25	20.0	16.0
	<b>MPU Physical Gate Length (nm)</b>	27	22	18.0	15.0	13.0
	<b>Wafer Overlay Control (nm) - 20% DRAM</b>	9.0	7.1	5.7	4.5	3.6
	<b>Wafer Overlay Control Double Patterning (nm)</b>	6	5	4	3	3
	<b>Lithography Metrology</b>					
Gate	Physical CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	2.8	2.3	1.9	1.6	1.3
	Wafer CD metrology tool <b>uncertainty</b> (3 $\sigma$ , nm) at P/T = 0.2	0.55	0.46	0.37	0.31	0.26
	Etched Gate Line Width Roughness (nm) <8% of CD	2.1	1.8	1.4	1.2	1.0
Dense Lines	Printed CD Control (nm) Allowed Litho Variance = 3/4 Total Variance	3.3	2.6	2.1	1.7	1.3
	Wafer CD metrology tool <b>uncertainty</b> (3s, nm) at P/T = 0.2	0.7	0.6	0.5	0.4	0.3
	<b>Double Patterning Overlay Metrology</b>					
	Double Exposure and Etch - Process Range (nm)	6.4	5.1	4.0	3.2	2.5
	Double Exposure and Etch - <b>Uncertainty</b> (nm)	1.3	1.0	0.8	0.6	0.5
	<b>Spacer PEE process</b>					
	First pass CD control (after etch) - Process Variation (nm)	3.0	2.4	1.9	1.6	1.3
	First pass CD control (after etch) - Uncertainty (nm)	0.6	0.5	0.4	0.3	0.3
	<b>Front End Processes Metrology</b>					
	High Performance Logic EOT equivalent oxide thickness (EOT), nm	0.65	0.5	0.5	0.5	0.5
	Logic Dielectric EOT Precision 3 $\sigma$ / #nm	0.0026	0.002	0.002	0.002	0.002
	<b>Interconnect Metrology</b>					
	Barrier layer thick (nm)	3.3	2.4	1.7	1.3	1.1
	Void Size for 1% Voiding in Cu Lines	4.5	3.6	2.8	2.3	
	Detection of Killer Pores at (nm) size	4.5	3.6	2.8	2.3	

# Lithography Metrology for Advanced Patterning

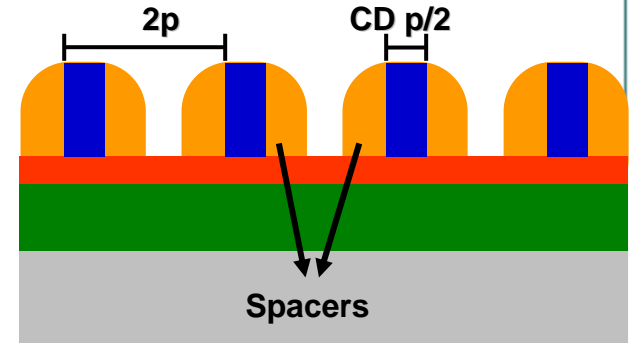
**Double Exposure**



**Double Patterning**



**Spacer Patterning**



**Metrology Need:**

**Latent Image CD**

**CD-AFM after both exposures but no Solution for CD between exposures**

**Metrology Need:**

**Overlay with Precision of 70% Of Single Layer**

**Metrology Need:**

**Spacer Thickness on Sidewall  
Spacer Profile**

**22 nm Dense lines**

# New Proposal for 2010 Test Structure Target Sizes

New lines for 2009/2010 ITRS in table MET3, by Bunday, based on ISMI Member Company feedback

<i>Year of Production</i>	<b>2010</b>	<b>2012</b>	<b>2014</b>	<b>2016</b>	<b>2018</b>	<b>2020</b>	<b>2022</b>	<b>2024</b>
<b>Flash ½ Pitch (nm) (un-contacted Poly)(f)</b>	<u>32</u>	<u>25</u>	<u>20</u>	<u>15.9</u>	<u>12.6</u>	<u>10.0</u>	<u>8.0</u>	<u>6.3</u>
<b>DRAM ½ Pitch (nm) (contacted)</b>	45	36	28	22.5	17.9	14.2	11.3	8.9
<b>Target Pad Size for OCD/scatterometry or Diffraction Overlay, or Target Size for Optical overlay (max size for either, square pad, size in microns)</b>	40	34	30	26	20	16	13	10
<b>In-die Micro-Targets for Overlay or OCD (target pad size in microns). Dimension includes all needed exclusion.</b>	10	10	5	2	2	2	2	2
<b>Move-Acquire-Measure Time for CD or Overlay (MAM time, seconds per measurement)</b>	1.0	1.0	0.9	0.7	0.7	0.5	0.5	0.5

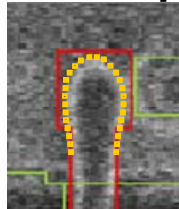


# Metrology Challenges for Advanced Litho Processes

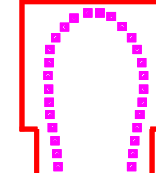
Double Exposure	Double Patterning	Spacer Double Patterning
<b>32/22 nm 1/2 Pitch</b>		
<b>For alignment need to measure latent image in</b>	<b>Sidewall Angle (SWA) and Height Accuracy for odd and</b>	<b>Spacer sidewall Thickness Uniformity across entire</b>
<p><b>2 Population CD, SWA, height and pitch</b></p> <p><b>Potential Solution -&gt; scatterometry</b></p> <p><b>Q: is there enough sensitivity for odd-even line scenario</b></p>		
	<b>Overlay at resolution (i.e. with targets at device size) : what is</b>	<b>SWA of odd and even lines</b>
	<p><b>Metrology for Latent Image at 1<sup>st</sup> exposure</b></p> <p><b>might be avoided using</b></p> <p><b>AEC/APC approaches &amp; CD/Overlay</b></p> <p><b>after double exposure</b></p>	
<b>Mask im</b>		<b>shape</b>
<b>M</b>		<b>uniformity</b>
		<b>er</b>
		<b>ormity</b>
	<b>mask CD uniformity metrology</b>	<b>Metrology</b>

# Contour Metrology

- For CD-SEMs, Design-Based Metrology (DBM) applications allow for practical SEM verification of design intent, through the collection of feature 2D contour shape information and comparison to GDS files.
  - automatic CD-SEM recipe setup from design information



Contour vs. GDS2



- DBM applications very important for development and verification of OPC
  - number of measurements for successfully developing OPC is expected to grow exponentially with technology generation.
  - metrology interfaces with the Design for Manufacturing (DFM) community.
- Contour fidelity is a prevailing challenge
  - Accuracy of contour extraction → strong implications for OPC
  - Accuracy of registration → strong implications for in-die overlay
- Remaining work : *define*:
  - contour error source testing methodologies
  - contour reference metrology
  - SEM modeling for contours



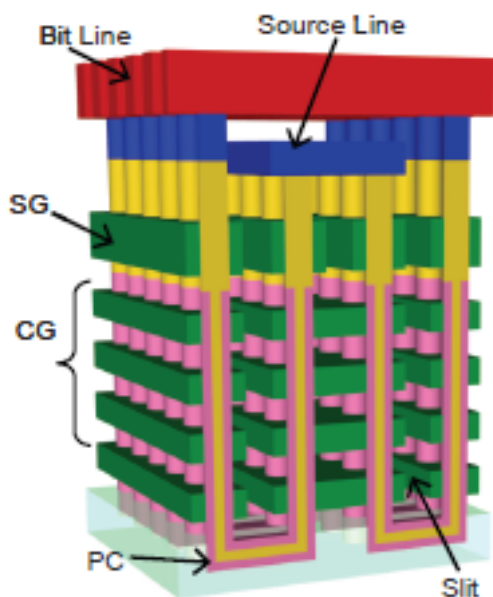
# FEP Metrology Gaps

- **New High K – Metal Gate Materials**
  - 3-D Profiling of Gates, Channel and S-D
- **III-V and SiGe Channels**
  - Defects
  - Lattice Misfits
  - Interfaces
- **New Memory Materials**
  - Phase Change Memory – polycrystalline chalcogenide)
  - Spintronic / Magnetic Films
    - CIPT needed
- **SOI**
  - Thickness down to 2nm
  - Defects in SOI layer
- **General**
  - 450mm wafers
  - 1.5mm EE
  - Wafer Flatness
  - Particles Detection
    - size, composition

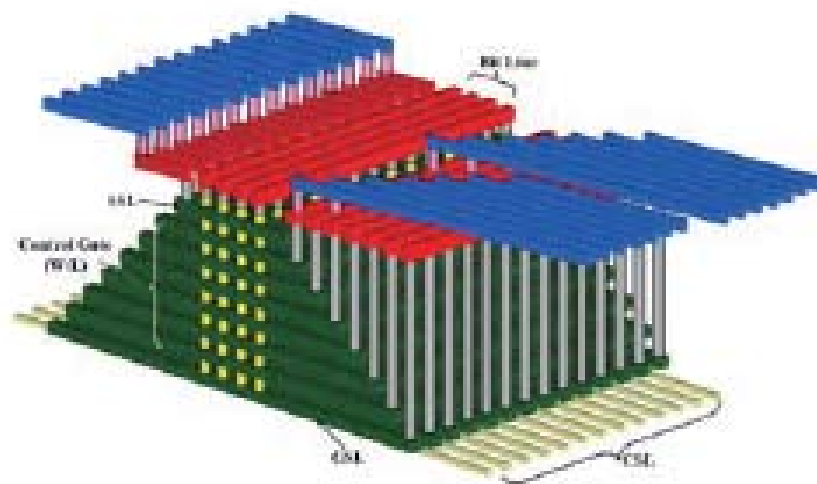
# FEP Metrology

3D Metrology – Complex structure measurement and inspection are required

e.g. high A/R holes, film thickness & properties on sidewall



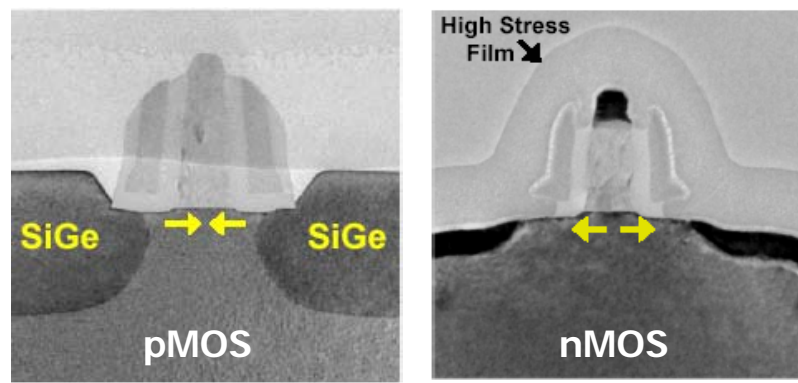
Pipe-shaped BiCS Flash Memory  
(R. Katsumata, Toshiba)



TCAT (Terabit Cell Array Transistor)  
(J. Jang, Samsung)

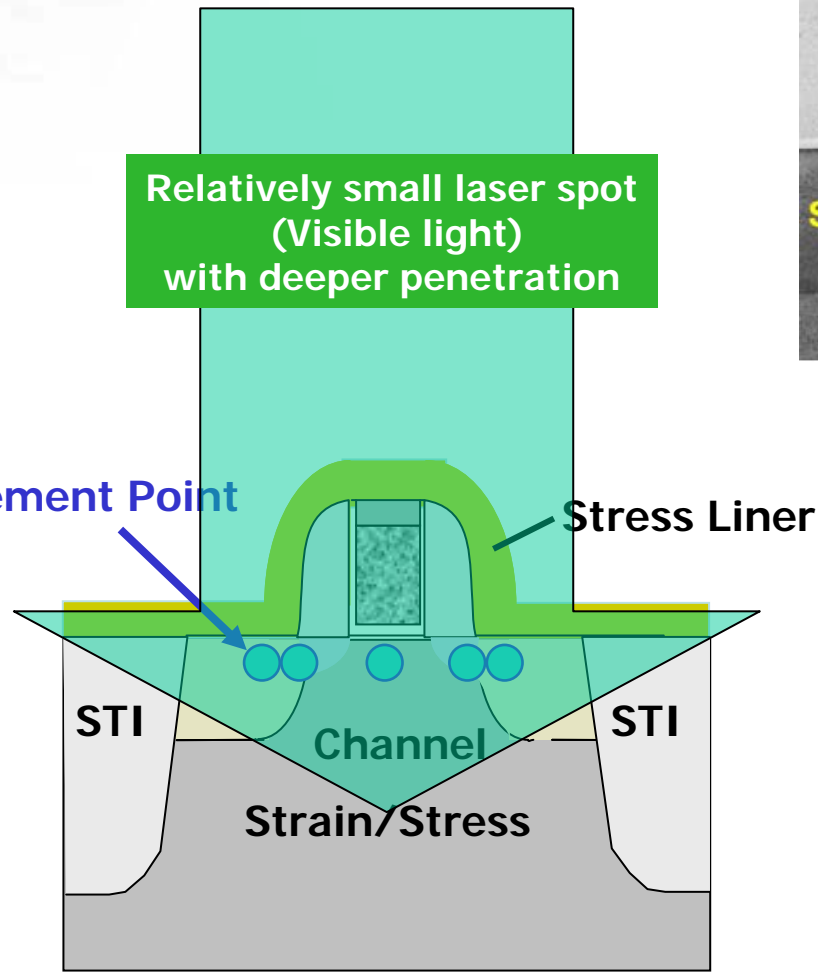
# Local Strain/Stress Measurement

Relatively small laser spot  
(Visible light)  
with deeper penetration

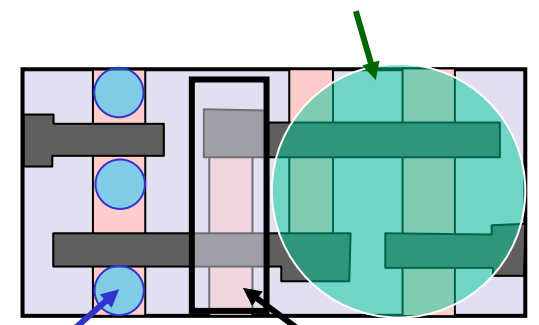


Ghani, et al (Intel)

Measurement Point



Wide laser spot  
for extracting average stress

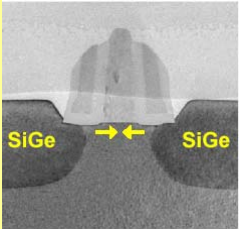

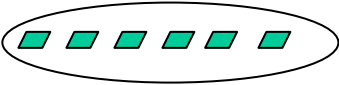



Small laser spot  
for extracting single Tr. stress

Cross sectioning  
for TEM



# Local Stress/Strain Measurement Method

Area of Interest	Measurement Method	Sensitivity Stress	Sensitivity Strain	Measurement Area	Sample Thickness	
<b>Transistor Level</b> 	- SEM EBSD					<b>Destructive</b>
	- CBED	20 MPa	0.02%	10-20nm	<100nm	<b>Destructive</b>
	- NBD	100 MPa	0.1%	~10nm	<300nm	<b>Destructive</b>
	- TERS	50 MPa	0.05%	<50nm		<b>Destructive</b>
<b>Micro-Area Level</b> 	- Confocal Raman	20 MPa	0.02%	~150nm		<b>Non-Destructive</b>
	- XRD	10 MPa	0.01%	100um		
	- Photo reflectance Spectroscopy	<20MPa	<0.02%	1um		<b>Non-Destructive</b>
<b>Die</b> 	- Die level flatness - Laser Interferometry - Coherent Gradient Sensing					<b>Non-Destructive</b>
<b>Wafer</b> 	- Laser Interferometry - Coherent Gradient Sensing					<b>Non-Destructive</b>

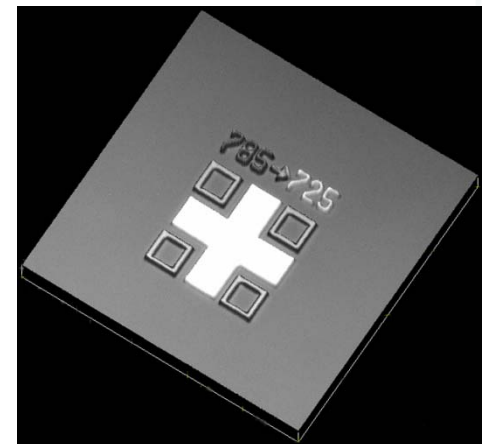
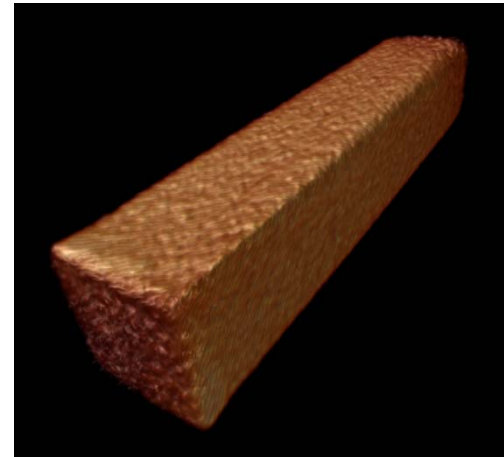


\* Stress – Strain relation : need to be clarified

TERS (Tip Enhanced Raman Scattering)  
 CBED (Convergent Beam Electron Diffraction)  
 NBD (Nano Beam Electron Diffraction)  
 XRD (X-ray Diffraction)

# 2009 Interconnect Metrology

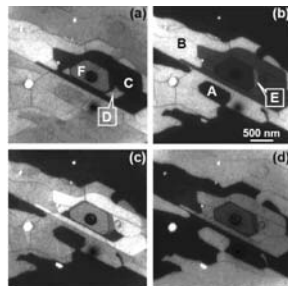
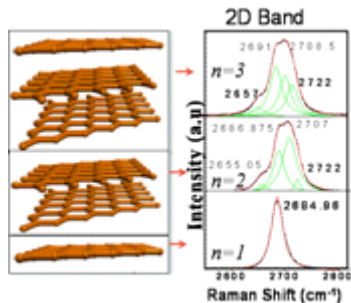
- Existing Challenges
  - Measurement Gap - Sidewall barrier thickness and sidewall damage (compositional changes in low k)
  - New - Porous low k is projected for 22 nm  $\frac{1}{2}$  Pitch
  - Detection of Voids after electroplating
  - Monolayer interface for new barrier-low k
- Air Gap sacrificial layer does not require unique metrology
- Metrology is needed for 3D Integration
  - TSV Depth and Profile through multiple layers
  - Alignment of chips for stacking – wafer level integration
  - Bond strength
  - Defects in bonding
  - Damage to metal layers
  - Defects in vias between wafers
  - Through Si via is high aspect ratio CD issue
  - Wafer thickness and TTV after thinning
  - Defects after thinning including wafer edge
- Emerging / Gated Interconnects
  - Native Device Interconnects



# Metrology for ERM/ERD

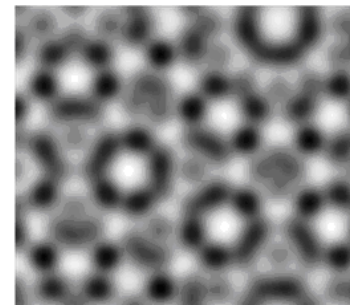
High carrier mobility and structural robustness have driven a considerable effort in Graphene research

How many Layers? Raman and LEEM

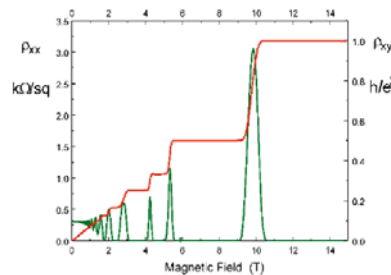
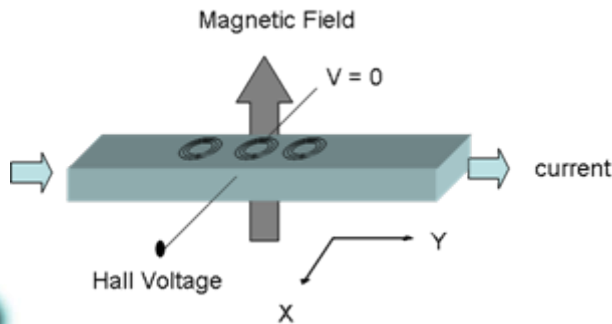


Measurement of Bi-layer  
misorientation

Aberration corrected TEM



Quantum Hall Effect observes the Berry Phase



# Metrology Summary

## • FEP-Interconnect-Litho

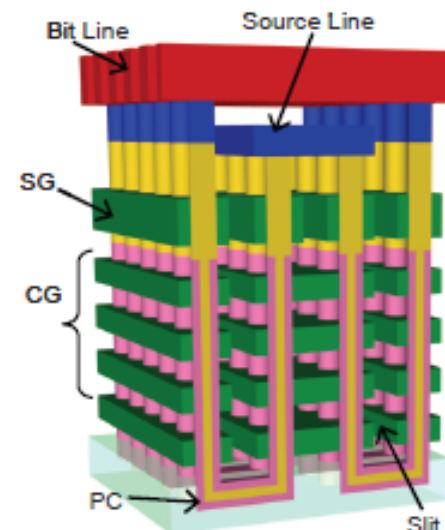
- PC and SST RAM - New materials for Metrology
- Dual Patterning
- 3D Metrology – Confirm Geometry Requirements e.g. film thickness & properties on sidewall
- Reference Methods for 3D
- Composition & Stress – e.g. buried channels
- EUV metrology requirements

## • ERD-ERM

- Standardization of Measurements
- Properties of low Dimensional Materials
- Microscopy and feature size/function
- Time resolved magnetic measurements
- Dimensional and Temporal Resolution of Local Structures and Dynamics

- Ability to perform real time measurements, e.g. phase transitions, transport properties, memory switching times, domain dynamics

## 3D Metrology for Advanced Memory



Graphene – C. Kisielowski

